

Notice of References Cited	Application/Control No. 09/823,148	Applicant(s)/Patent Under Reexamination YOUNGS ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,070,252	05-2000	Xu et al.	714/30
	B	US-5,355,369	10-1994	Greenberger et al.	714/727
	C	US-6,122,762	09-2000	Kim, Ho-Ryong	714/726
	D	US-4,969,148	11-1990	Nadeau-Dostie et al.	714/718
	E	US-6,404,684	06-2002	Arimoto et al.	365/201
	F	US-5,254,942	10-1993	D'Souza et al.	714/727
	G	US-6,070,256	05-2000	Wu et al.	714/718
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Designing Dual Personality IEEE 1149.1 Compliant Multi-Chip Modules", Najmi Jarwala, 1994, IEE International Test Conference 1994, paper 19.3, pp 446-455.
	V	"Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International , 3-5 Oct. 2000, pp 628 -637.
	W	"Testability, Debuggability, and Manufacturability Features of the UltrSPARC-I Microprocessor", Levitt et al., 1995, International Test Conference 1995, paper 6.2, pp 157-166.
	X	"A 5 GB/s 9-Port Application Specific SRAM with Built-in Self Test", Wood et al., 1995 International Workshop on Memory Technology, Design and Testing, 1995, 7-8 Aug 1995, pp 68-73.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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*	U	"IEE Standard Test Access Port and Boundary Scan Architecture", 1990, IEEE Standard 1149.1
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